C1

b. an asynchronous portion coupled with a line for the memory cell; and

Cont -

c. a feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion and resetting the decoder in response to an asynchronous reset signal independent of the clocked signal.

REMARKS

A petition for a two-month extension of time and a request for continued examination accompany this Amendment C.

Responding to section (A) of the Advisory Action, the undersigned did not receive page 2 of the January 29, 2003 Office Action until the Examiner sent it via facsimile on May 30, 2003. The applicants thank the Examiner for sending the missing page. The applicants respectfully traverse the rejection of claims 1-2 and 4 under 35 U.S.C. 112, first paragraph. Claim 1 has been amended to recite "A decoder for a memory cell responsive to an address comprising:" The decoder shown in Fig. 8 is responsive to the output of global word decoders, such as 620a-620d, shown in Fig. 6. The global word decoders, in turn, are responsive to a predecoder 622 that transmits address information. (See Fig. 6 and page 26, lines 24-34.) Thus, a decoder that is responsive to an address, as claimed, is supported by the disclosure.

Responding to section (B) of the Advisory Action, the rejection of claims 1-2 and 4 under 35 U.S.C. 102(b) as being anticipated by Becker et al. (U.S. Patent No. 5,886,929, "Becker") is respectfully traversed. Amended claim 1 reads (emphasis supplied):

1. (Three Times Amended) A decoder for a memory cell responsive to an address comprising:

a. a synchronous portion disposed to receive and respond to a clocked signal;

b. an asynchronous portion coupled with a line for the memory cell; and

c. a feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion and resetting the decoder in response to an asynchronous reset signal independent of the clocked signal.

The amendments to claim 1 are supported by the embodiments described in Fig. 8 and described on page 32, line 10 – page 33, line 9.

Becker does not teach or suggest at least the underlined portions of amended claim 1. As explained on page 32, lines 14-16, "[I]t is desirable that the word line be reset independently of the clock and also of the varying of the input signals to the word line decoder." Becker neither teaches nor suggests such a feature. As a result, claim 1 is allowable over Becker.

Amended claim 1 also is patently distinguishable from Tomita (U.S. Patent No. 5,886,941 cited against claim 1 in the September 16, 2002 Office Action. In that Office Action, the Examiner took the position that the reset signal R from the output of gate 105 is an asynchronous signal (page 4). The applicants respectfully traverse that position. In any event, the output of gate 105 is not independent of a clock signal as claimed. For all the foregoing reasons, claim 1 also is patentable over Tomita.

Claims 2 and 4 are dependent on claim 1 and are allowable for the same reasons as claim 1.

Claims 6-10 and 12-16 were allowed in the January 29, 2003 Office Action.

In summary, each of claims 1-2, 4, 6-10 and 12-16 is allowable, and such action is respectfully requested.

The undersigned requests that the Examiner telephone the undersigned and arrange for a telephone interview regarding this application.

Date: June 18, 2003

Respectfully submitted,

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1. (Three Times Amended) [An address] A decoder for a memory cell[,] responsive to an address comprising:

a. a synchronous portion[,] disposed to receive and respond to a clocked signal;

b. an asynchronous portion[,] coupled with a line for the memory cell; and

c. a feedback-resetting portion [comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, the feedback-resetting portion] substantially isolating the synchronous portion from the asynchronous portion [responsive] and resetting the decoder in response to an asynchronous reset signal independent of the clocked signal.